Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A MOS transistor, comprising:

a gate structure formed over a semiconductor;

source and drain regions formed in said semiconductor;

drain and source extension regions formed in said semiconductor adjacent said gate structure and positioned between said gate structure and said source and drain regions; ~~and~~

first metal silicide layers formed on said drain and source extension regions~~.~~ ;

sidewall structures adjacent said gate structure and over said first metal silicide layers; and

second metal silicide layers formed on said source and drain regions.

Claim 2 (currently canceled)

Claim 3 (currently canceled)

Claim 4 (original): The MOS transistor of claim 1 wherein said first metal silicide layer is selected from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

Claim 5 (original): The MOS transistor of claim 2 wherein said drain and source extension regions have a first doping concentration and said drain and source regions have a second doping concentration such that said second doping concentration is greater than said first doping concentration.

Claim 6 (original): The MOS transistor of claim 5 wherein said drain and source extension regions extend to a first depth and said drain and source regions extend to a second depth such that said second depth is greater than said first depth.

Claim 7 (original): An integrated circuit MOS transistor, comprising:

a gate structure formed over a semiconductor;

sidewall structures formed adjacent said gate structure;

a semiconductor layer formed above said semiconductor adjacent to said sidewall structure;

source and drain regions formed adjacent to said sidewall structures in said semiconductor layer and said semiconductor;

drain and source extension regions formed in said semiconductor adjacent said gate structure and positioned substantially beneath said sidewall structures; and

first metal silicide layers formed on said drain and source extension regions.

Claim 8 (original): The MOS transistor of claim 7 further comprising second metal silicide layers formed on said source and drain regions.

Claim 9 (original): The MOS transistor of claim 7 wherein said first metal silicide layer is selected from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

Claim 10 (original): The MOS transistor of claim 7 wherein said drain and source extension regions have a first doping concentration and said drain and source regions have a second doping concentration such that said second doping concentration is greater than said first doping concentration.

Claim 11 (original): The MOS transistor of claim 10 wherein said drain and source extension regions extend to a first depth and said drain and source regions extend to a second depth such that said second depth is greater than said first depth.

Claim 12 (currently amended): A method for forming a MOS transistor, comprising:

forming a gate structure over a semiconductor;

forming source and drain regions in said semiconductor;

forming drain and source extension regions in said semiconductor adjacent said gate structure and positioned between said gate structure and said source and drain regions; ~~and~~

forming first metal silicide layers on said drain and source extension regions~~.~~;

forming sidewall structures adjacent said gate structure and over said first metal silicide layers; and

forming second metal silicide layers on said source and drain regions.

Claim 13 (currently canceled):

Claim 14 (currently canceled):

Claim 15 (original): The method of claim 12 wherein said first metal silicide layer is formed from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

Claim 16 (original): The method of claim 12 wherein said drain and source extension regions are formed using with a first doping concentration and said drain and source regions are formed using a second doping concentration such that said second doping concentration is greater than said first doping concentration.

Claim 17 (original): The method of claim 16 wherein said drain and source extension regions are formed to extend to a first depth and said drain and source regions extend to a second depth such that said second depth is greater than said first depth.

Claim 18 (original): An integrated circuit MOS transistor, comprising:

forming a gate structure over a semiconductor;

forming sidewall structures adjacent said gate structure;

forming a semiconductor layer above said semiconductor adjacent to said sidewall structure;

forming source and drain regions adjacent to said sidewall structures in said semiconductor layer and said semiconductor;

forming drain and source extension regions in said semiconductor adjacent said gate structure and positioned substantially beneath said sidewall structures; and

forming first metal silicide layers on said drain and source extension regions.

Claim 19 (original): The method of claim 18 further comprising forming second metal silicide layers on said source and drain regions.

Claim 20 (original): The method of claim 18 wherein said first metal silicide layer is formed from the group consisting of cobalt silicide, nickel silicide, titanium silicide, and tungsten silicide.

Claim 21 (original): The method of claim 18 wherein said drain and source extension regions are formed with a first doping concentration and said drain and source regions are formed with a second doping concentration such that said second doping concentration is greater than said first doping concentration.

Claim 22 (original): The method of claim 21 wherein said drain and source extension regions are formed to a first depth and said drain and source regions are formed to a second depth such that said second depth is greater than said first depth.